REMARKS/ARGUMENTS

Applicants acknowledge the rejection of claims 1, 2, 4-10, 12 and 14-23 with a right to traverse. Applicants respectfully request further examination and reconsideration of the rejections for the reasons stated below.

Claim Rejections - 35 U.S.C. §103

Independent claims 1, 10 and 12 were rejected as being unpatentable over U.S. Patent No. 5,371,878 (hereinafter "Coker") in view of "How Debuggers Work" by Jonathan B. Rosenberg (hereinafter "Rosenberg) and further in view of U.S. Patent No. 5,968,135 (hereinafter "Teramoto"). Applicants respectfully traverse in view of the following.

Claim 1 recites a boot method for synchronizing a microcontroller and a virtual microcontroller of an In-Circuit Emulation system in lock step through executing a set of boot code in the microcontroller and executing a dummy code in the virtual microcontroller, wherein the dummy code is a set of timing code to take the same number of clock cycles as the microcontroller and wherein the set of boot code is inaccessible to the virtual microcontroller, as claimed.

The rejection states that Cocker teaches the features of executing a set of timing code to enable the lock-step synchronization in a virtual microcontroller, as claimed. In support of the rejection, the Examiner cites that "[a] shadow system of this invention executes the same software as the target-ECS from system start-up or reset," See Column 2, Lines 56-58 and "[t]he shadow system and the target-ECS function exactly the same except that the shadow system receives data slightly delayed because of a data buffer between the target-ECS and the shadow system," See Column 3, Lines 13-16. However, according to the citations, Coker fails to teach or suggest the claimed features that during the booting process, the microcontroller executes the set of boot code, whereas the virtual microcontroller executes the set of timing code. Unlike Cocker where the same software is used for both the target-ECS and shadow system during the start up, Claim 1 recites the features that the microcontroller (which corresponds to the target-ECS in Cocker) and the virtual microcontroller (which corresponds to the shadow system) do not run the same software. Since Cocker fails to teach or suggest the claimed features, Applicants respectfully submit that Claim 1 is in condition for allowance.

The rejection further states that Cocker teaches the features that the set of boot code is stored within the microcontroller and the set of boot code is inaccessible to the virtual microcontroller, as claimed. Applicants understand that Cocker is not explicit on the features. However, from Cocker's teaching that "[a] shadow system of this invention executes the same software as the target-

ECS from system start-up or reset," See Column 2, Lines 56-58, one skilled in the art can infer that both the target-ECS and the shadow system execute the same boot code during the start up. Therefore, Cocker at least does not teach the claimed features that the virtual microcontroller, which executes the timing code, cannot access the boot code during the start up, as claimed. Since Cocker fails to teach or suggest the claimed features, Applicants respectfully submit that Claim 1 is in condition for allowance.

Moreover, the rejection states that Teramoto teaches the claimed features that the dummy code is a set of timing code to take the same number of clock cycles as the microcontroller. In support of the rejection, the Examiner cites passages In Teramoto that "[t]he present invention relates to an instruction execution control method and information processing information apparatus for monitoring information about the completion of synchronization between processors, and selectively causing a specific instruction of the subsequent group of Instructions to wait until the completion of synchronization is indicated when the processors are operated in synchronism with each other for synchronous execution of their respective processes in a computer system including a plurality of processors," See Column 1, Lines 7-16, and that "[w]hen the instruction, which was read out, is a wait instruction, the instruction analyzer 102 issues a wait instruction to the wait instruction controller 100 through the interface signal 105" where "[t]he wait instruction controller 100 executes the wait

instruction which controls the instruction execution sequence according to the present invention," See Column 5, Lines 50-60.

However, Applicants respectfully submit that no where in Teramoto teaches or suggests the features that during the booting process, the virtual microcontroller runs dummy code where the dummy code is a set of timing code to take the same number of clock cycles as the microcontroller, as claimed. Applicants understand that there is no mention of "dummy code" in Teramoto. Teramoto instead teaches of issuing a wait instruction using a wait instruction controller which inhibits next instruction ("the Load instruction) from sent to the execution, See Column 5, Lines 54-60. Thus, Teramoto teaches at most a different method or a system of synchronizing processors during their real time operations. Accordingly, Applicants respectfully submit that Teramoto fails to teach the features of synchronizing a microcontroller and a virtual microcontroller by executing a boot code and a dummy timing code, respectively, during the booting process, as claimed. Since Cocker fails to teach or suggest the claimed features, Applicants respectfully submit that Claim 1 is in condition for allowance.

Independent claims 10 and 12 recite at least the those features similar to that of Claim 1 and are therefore patentable over the cited references for the same reasons. As such, allowance of independent Claims 10 and 12 is earnestly solicited.

With respect to remaining Claims that depend on Claims 1, 10 and 12, Applicants respectfully assert that the Claims overcome the rejections of record for at least the rationale previously presented with respect to the independent Claims, and respectfully solicit allowance of these Claims.

In particular, Claim 22 is rejected under 35 USC 103(a) as being unpatentable over Coker in view of Rosenberg, further in view of Teramoto as applied to Claim 1 and further in view of U.S. Patent No. 4,757,534 (hereinafter "Matyas"). With respect to Claim 22, Applicants respectfully assert that Rosenberg, Coker, Matyas or their combination fails to teach or suggest the limitation of "the boot code containing algorithms." The rejection states that Matyas teaches code that comprises serial number, passwords, and algorithms "[i]n carrying out the computer/smart card protocol, the T output is sent to the smart card together with the parameter P1 (password) and P2 (programming number | diskette serial number, where | denotes concatenation) and a third parameter P3" where P3 is the computer number and the DES algorithm is used to encrypt the file key.

Although Matyas teaches the passing of serial number and password as a part of the code being passed, the reference does not teach that any algorithm is contained in the code being passed. The third parameter P3 being passed is a computer number interpreted by the DES algorithm, See Column 13, Lines 13-15. Matyas does not teach that the DES algorithm, or any other algorithm, is

passed along with the serial number and password as a part of the code. For this additional reason, Applicants respectfully assert that Claim 22 overcomes the rejections of record, and respectfully solicit allowance of this Claim.

For the reasons stated above, Applicants earnestly solicit the allowance of Claims 1, 2, 4-10, 12 and 14-23.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-2, 4-10, 12 and 14-23 overcome the rejections of record and, therefore, allowance of Claims 1-2, 4-10, 12 and 14-23 is earnestly solicited.

Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,

Murabito, Hao & Barnes LLP

Date 4/28/2008

By _____

Steve S. Ko
Reg. No. 58,757

Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060